

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Dureseti Chidambarao, et al.

Group Art Unit: Unknown

Serial No.: Not assigned yet

Examiner: unknown

Filed: Concurrently herewith

**For: STRAINED DISLOCATION-FREE CHANNELS FOR CMOS AND METHOD OF
MANUFACTURE**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. 1.56**

Sir:

Under provisions of 37 C.F.R. 1.97 through 1.99 and pursuant to applicant's duty of disclosure under 37 C.F.R. 1.56, applicants respectfully bring the document listed on the attached Form PTO-1449 to the attention of the Examiner in charge of the above-identified application. A copy of the cited documents (non US patents) is enclosed for the convenience of the Examiner.

This citation does not constitute an admission that the cited references are relevant or material to the claims nor should it be construed as a representation that no other art than that identified exists. They are merely cited as constituting related art of which the applicant is aware.

It is respectfully requested that this documents be considered by the Examiner and formally made of record in this application.

Respectfully submitted,



Andrew M. Calderon
Reg. No. 38,093

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1750 Tysons Boulevard, Suite 1800
McLean, VA 22102
(703)712-5000

FORM PTO-1449 (Modified)	ATTY. DOCKET NO. FIS9-2003-0244US1	SERIAL NO. Unassigned
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	APPLICANT: Dureseti Chidambarao, et al.	
(Use several sheets if necessary)	FILING DATE: Concurrently Herewith	GROUP: Unassigned

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
	6,228,694 B1	5/8/2001	Doyle et al.			
	6,406,973 B1	6/18/2002	Lee			
	6,281,532 B1	8/28/2001	Doyle et al.			
	5,683,934	11/4/97	Candelaria			
	6,368,931 B1	4/9/2002	Kuhn, et al.			
	5,310,446	5/10/94	Konishi et al.			
	4,853,076	8/1/89	Tsaur et al.			
	US 2002/0090791 A1	7/11/2002	Doyle et al.			
	US 2002/0074598 A1	6/20/2002	Doyle et al.			
	6,509,618 B2	7/21/2003	Jan et al.			
	6,476,462 B2	11/5/2002	Shimizu et al.			
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	6,228,694 B1	5/8/2001	Doyle et al.			
	5,565,697	10/15/96	Asakawa et al.			
	US 2003/0040158 A1	2/27/2003	Saitoh			
	US 2002/0086472 A1	7/4/2002	Roberds et al.			
	6,521,964 B1	2/18/2003	Jan et al.			
	6,506,652	01/14/03	Jan, et al.			

FOREIGN PATENT DOCUMENTS

DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
					YES	NO

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

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		5,081,513	1/14/1992	Jackson, et al.			
		3,602,841	8/31/1971	McGroddy			
		6,531,740	3/11/2003	Bosco, et al.			
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		6,501,121	12/31/2002	Yu, et al.			
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		6,361,885	3/26/2002	Chou			
		6,255,169	7/3/2001	Li, et al.			
		6,246,095	6/12/2001	Brady, et al.			
		6,165,383	12/26/2000	Chou			
		6,133,071	10/17/2000	Nagai			
		6,046,464	4/4/2000	Schetzina			
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	5,940,736	8/17/1999	Brady, et al.			
	5,880,040	3/9/1999	Sun, et al.			
	5,861,651	1/19/1999	Brasen, et al.			
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	5,471,948	12/5/1995	Burroughes, et al.			
	5,459,346	10/17/1995	Asakawa, et al.			
	5,391,510	2/21/1995	Hsu, et al.			
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	5,108,843	4/28/1992	Ohtaka, et al.			
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		6,284,626	9/4/2001	Kim			
		6,274,444	8/14/2001	Wang			
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	5,557,122	9/17/1996	Shrivastava, et al.			
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	4,952,524	8/28/1990	Lee, et al.			
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	2002/0086497	07-04-2002	Kwok			
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	6,403,486	06-11-2002	Lou			
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	2003/0067035	04-10-2003	Tews et al.			
	6,461,936	10-08-2002	von Ehrenwall			
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	2001/0009784	07-26-2001	Ma et al.			

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	Kern Rim, et al., "Transconductance Enhancement in Deep Submicron Strained-Si <i>n</i> -MOSFETs", International Electron Devices Meeting, 26, 8, 1, IEEE, September 1998.
	Kern Rim, et al., "Characteristics and Device Design of Sub-100 nm Strained Si N- and PMOSFETs", 2002 Symposium On VLSI Technology Digest of Technical Papers, IEEE, pp 98-99.
	Gregory Scott, et al., "NMOS Drive Current Reduction Caused by Transistor Layout and Trench Isolation Induced Stress", International Electron Devices Meeting, 34.4.1, IEEE, September 1999.
	F. Ootsuka, et al., "A Highly Dense, High-Performance 130nm node CMOS Technology for Large Scale System-on-a-Chip Application", International Electron Devices Meeting, 23.5.1, IEEE, April 2000.
	Shinya Ito, et al., "Mechanical Stress Effect of Etch-Stop Nitride and its Impact on Deep Submicron Transistor Design", International Electron Devices Meeting, 10.7.1, IEEE, April 2000.
	A. Shimizu, et al., "Local Mechanical-Stress Control (LMC): A New Technique for CMOS-Performance Enhancement", International Electron Devices Meeting, IEEE, March 2001.
	K. Ota, et al., "Novel Locally Strained Channel Technique for high Performance 55nm CMOS", International Electron Devices Meeting, 2.2.1, IEEE, February 2002.

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